09-27-00 A

EXPRESS MAIL LABEL NO. EL379159911US

Attorney Docket No. 72255/02661

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s) : Kenneth W. Batcher

For (title) : DIRECT DATA ROUTING SYSTEM

1. Type of Application

This new application is for a(n):

(X) Original (nonprovisional)
( ) Continuation
( ) Continuation-in-part (CIP)
( ) Divisional
( ) Design
( ) Plant

NOTE: If continuation, CIP or divisional, then complete section 2.

CERTIFICATION UNDER 37 C.F.R. 1.10*
(Express Mail label number is mandatory.)
(Express Mail certification is optional.)

I hereby certify that this New Application Transmittal and the documents referred to as attached therein are being deposited with the United States Postal Service on this date September 26, 2000, in an envelope as "Express Mail Post Office to Addressee," mailing Label Number EL379159911US, addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231.

Valerie A. Milam

Valerie A. Milam

Signature of person mailing paper

WARNING: *Certificate of mailing (first class) or facsimile transmission procedures of 37 C F R. 1.8 cannot be used to obtain a date of mailing or transmission for this correspondence.*

****WARNING:*** *Each paper or fee filed by "Express Mail" **must** have the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 C.F.R. 1.10(b).*

2. Benefit of Prior U.S. Application(s) (35 U.S.C. 119(e), 120, or 121)

NOTE: If the new application being transmitted is a continuation, CIP or divisional, of a parent case, or where the parent case is an International Application which designated the U.S., or the benefit of a prior **provisional** application is claimed, then check the following item and complete section as follows.

() The new application being transmitted claims the benefit of prior U.S. application(s).

2.1 Relate Back

WARNING: If an application claims the benefit of the filing date of an earlier filed application under 35 U.S.C. 120, 121 or 365(c), the 20-year term of that application will be based upon the filing date of the earliest U.S. application that the application makes reference to under 35 U.S.C. 120, 121 or 365(c). (35 U.S.C. 154(a)(2) does not take into account, for the determination of the patent term, any application on which priority is claimed under 35 U.S.C. 119, 365(a) or 365(b).) For a CIP application, applicant should review whether any claim in the patent that will issue is supported by an earlier application and, if not, the applicant should consider canceling the reference to the earlier filed application. The term of a patent is not based on a claim-by-claim approach. See Notice of April 14, 1995, 60 Fed Reg. 20,195, at 20,205.

(complete the following, if applicable)

Amend the specification by inserting, before the first line, the following sentence:

A. 35 U.S.C. 120, 121 and 365(c)

() "This is a
- ( ) continuation
- ( ) continuation-in-part
- ( ) divisional

of copending application(s) serial number filed on ."

( ) International Application_____ filed on_____ and which designated the U.S."

Note: The proper reference to a prior filed PCT application that entered the U.S. national phase is the U.S. serial number and the filing date of the PCT application that designated the U.S. Moreover, (1) Where the application being transmitted adds subject matter to the International Application, then the filing can be as a continuation-in-part or (2) if it is desired to do so for other reasons then the filing can be as a continuation.

( ) "The nonprovisional application designated above, namely application no._____, filed_____, claims the benefit of U.S. Provisional Application(s) No(s).:

{list application no(s). and filing date(s)}

B. 35 U.S.C. 119(e) (Provisional Application)

( ) "This application claims the benefit of U.S. Provisional Application(s) No(s).:

{list application no(s). and filing date(s)}

2.2 Relate Back—35 U.S.C. 119 Priority Claim for Prior Application

The prior U.S. application(s), including any prior International Application designating the U.S., identified above in item 2.1(A), in turn itself claim(s) foreign priority(ies) as follows:

{list country, application no(s). and filing date(s)}

The certified copy(ies) has (have)

( ) been filed on_____, in prior application serial no.____, which was filed on___.

( ) is (are) attached.

2.3 Maintenance of Copendency of Prior Application

NOTE: The PTO finds it useful if a copy of the petition filed in the prior application extending the term for response is filed with the papers constituting the filing of the continuation application Notice of November 5, 1985 (1060 O.G. 27).

A. ( ) Extension of time in prior application

*(This item **must** be completed and the papers filed **in the prior application** if the period set in the prior application has run.)*

( ) A petition, fee and response extends the term in the pending **prior** application until Extension of_____.

( ) A **copy** of the petition filed in prior application is attached.

B. ( ) Conditional Petition for Extension of Time in Prior Application

(complete this item, if previous item not applicable)

( ) A conditional petition for extension of time is being filed in the pending **prior** application.

( ) A **copy** of the conditional petition filed in the prior application is attached.

2.4 Further Inventorship Statement Where Benefit of Prior Application(s) Claimed

(complete applicable item A, B and/or C below)

A. ( ) This application discloses and claims only subject matter disclosed in the prior application whose particulars are set out above, and the inventor(s) in this application are

( ) the same.

( ) less than those named in the prior application. It is requested that the following inventor(s)

identified for the prior application be deleted:

{ type name(s) of inventor(s) to be deleted }

B. ( ) This application discloses and claims additional disclosure by amendment and a new declaration or oath is being filed. With respect to the prior application, the inventor(s) in this application are

( ) the same.

( ) the following additional inventor(s) have been added:

(type name(s) of inventor(s) to be added)

C. ( ) The inventorship for all the claims in this application are

( ) the same.

( ) not the same. An explanation, including the ownership of the various claims at the time the last claimed invention was made

( ) is submitted.

( ) will be submitted.

2.5 Abandonment of Prior Application *(if applicable)*

( ) Please abandon the prior application at a time while the prior application is pending, or when the petition for extension of time or to revive In that application is granted, and when this application is granted a filing date, so to make this application copending with said prior application.

NOTE: According to the Notice of May 13, 1983 (103, TMOG 6-7), the filing of a continuation or continuation-in-part application is a proper response with respect to a petition for extension of time or a petition to revive and should include the express abandonment of the prior application conditioned upon the granting of the petition and the granting of a filing date to the continuing application.

2.6 Petition for Suspension of Prosecution for the Time Necessary to File an Amendment

NOTE· Where it is possible that the claims on file will give rise to a first action final for this continuation application and for some reason an amendment cannot be filed promptly (e.g, experimental data is being gathered) it may be desirable to file a petition for suspension of prosecution for the time necessary.

(check the next Item, if applicable)

( ) There is provided herewith a Petition To Suspend Prosecution for the Time Necessary to File An Amendment (New Application Filed Concurrently)

2.7 Small Entity (37 CFR § 1.28(a))

( ) Applicant has established small entity status by the previous submission of a statement in prior application serial no.____ on ____.

( ) A copy of the statement previously filed is included.

WARNING: See 37 CFR § 1.28(a).

2.8. Notification in Parent Application of this Filing

( ) A notification of the filing of this
(check one of the following)

( ) continuation
( ) continuation-in-part
( ) divisional

is being filed in the parent application, from which this application claims priority under 35 U.S.C. § 120.

2.9 Incorporation by Reference

() the entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

3. Papers Enclosed Which are Required for Filing Date Under 37 CFR 1.53(b) (Regular) or 37 CFR 1.153 (Design) Application

(x) 14 Pages of specification
(x) 8 Pages of claims
(x) 1 Pages of Abstract
(x) 3 Sheets of drawing
(x) formal
() informal

4. Additional papers enclosed

() Amendment to claims:

( ) **Cancel** in this application claims_____ before calculating the filing fee. (At least one original independent claim must be retained for filing purposes).

( ) **Add** the claims shown in the attached amendment. (Claims added have been numbered consecutively following the highest numbered original claims).

( ) Preliminary Amendment
( ) Information Disclosure Statement (37 C.F.R. 1.98)
( ) Form PTO-1449
( ) Citations
( ) Declaration of Biological Deposit
( ) Special Comments
( ) Other

5. Declaration or oath (including power of attorney)

(x) ENCLOSED.
(x) Newly executed (original or copy)
() Copy from prior application No. 0 / _____ (37 CFR 1.63(d)- continuation/divisional)

( ) DELETION OF INVENTOR(S) - signed statement attached deleting inventor(s) named in the above-noted prior application (37 CFR 1.63(d) and 1.33(b))

Declaration or Oath executed by: (check **all** applicable boxes)
(x) inventor(s).
( ) legal representative of inventor(s). 37 CFR 1.42 or 1.43
( ) joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.
( ) this is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is also attached. See item 13 below for fee.

() NOT ENCLOSED.
( ) Application is made by a person authorized under 37 CFR 1.41(c) on behalf of all the above named inventor(s). The declaration or oath, along with the surcharge required by 37 CFR 1.16(e) can be filed subsequently.
( ) Showing that the filing is authorized. (Not required unless called into question. 37 CFR 1.41(d)).

6. Inventorship Statement

WARNING: If the named inventors are each not the inventors of all the claims an explanation, including the ownership of the various claims at the time the last claimed invention was made, should be submitted.

The inventorship for all the claims in this application are:
() The same
or
() Not the same. An explanation, including the ownership of the various claims at the time the last

claimed invention was made,

() is submitted

() will be submitted.

7. Language

(x) English

() Non-English

() the attached translation is a verified translation. 37 CFR 1.52(d).

8. Assignment

(x) An assignment of the invention to Cisco Technology, Inc.

(x) is attached. (A separate "ASSIGNMENT COVER LETTER ACCOMPANYING NEW PATENT APPLICATION" is also attached.)

() will follow.

() The prior application is assigned of record to __(copy attached).

9. Certified Copy - Foreign Priority Claim Under 35 U.S.C. 119

Certified copy(ies) of application(s)

{list country, application no(s). and filing date(s)}

from which priority is claimed

() is (are) attached.

() will follow.

NOTE: The foreign application forming the basis for the claim for priority **must** be referred to in the **oath** or **declaration**. 37 CFR 1.55(a) and 1.63.

NOTE: This item is for any foreign priority for which the application being filed directly relates. If any parent U.S application or International Application form which this application claims benefit under 35 U.S.C. 120 is itself entitled to priority from a prior foreign application then complete item 17 on the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OR PRIOR U.S. APPLICATION(S) CLAIMED.

10. Fee Calculation (37 C.F.R. 1.16)

A. (x) Regular Application

CLAIMS AS FILED				
	Number Filed	Number Extra	Rate	Basic Fee $690.00

Total Claims (37 CFR 1.16(c))	41 - 20 =	21	x $ 18.00	$ 378
Independent Claims (37 CFR 1.16(b))	11 - 3 =	8	x $ 78.00	$ 624
Multiple dependent claim(s), if any (37 CFR 1.16(d))	0	0	+ $ 260.00	$ 0.00

( ) Amendment canceling extra claims enclosed.
( ) Amendment deleting multiple dependencies enclosed.
( ) Fee for extra claims is not being paid at this time.

NOTE: If the fees for extra claims are not paid on filing they must be paid or the claims canceled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency. 37 CFR 1.16(d).

Filing Fee Calculation $ 1,692.00

B. () Design Application
($330.00 - 37 CFR 1.16(f))

Filing Fee Calculation $

11. Small Entity Statement(s)

() Verified Statement(s) that this is a filing by a small entity under 37 CFR 1.9 and 1.27 is(are) attached.

Filing Fee Calculation (50% of **A** or **B** above) $

NOTE: Any excess of the full fee paid will be refunded if a verified statement and a refund request are filed within **2 months** of the date of timely payment of a full fee. 37 CFR 1.28(a).

12. Request for International-Type Search (37 C.F.R. 1.104(d))

( ) Please prepare an international-type search report for this application at the time when national examination on the merits takes place.

13. Fee Payment Being Made At This Time

( ) NOT ENCLOSED.
( ) No filing fee is to be paid at this time. (This and the surcharge required by 37 CFR 1.16(e) can be paid subsequently.)

(x) ENCLOSED

(x) Filing fee $ 1,692.00

(x) Recording assignment
($40.00; 37 CFR 1.21(h)(1)) $ 40.00

( ) petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached. ($130.00; 37 CFR 1.47 & 1.17(h))
$____

( ) for processing an application with a specification is a non-English language. ($130.00 37 CFR 1.52(d) and 1.17(k))
$____

( ) processing and retention fee. ($130.00; 37 CFR 1.53(d) and 1.21(l))
$____

( ) Fee for international-type search report. ($40.00; 37 CFR 1.21(e))
$____

Total fees enclosed **$ 1,732.00**

14. Method of Payment of Fees

(x) Check in the amount of $ 1,732.00

() Charge Account No. 50-0902 in the amount of $ A duplicate of this transmittal is attached.

15. Authorization to Charge Additional Fees

WARNING: If no fees are to be paid on filing the following items should **not** be completed.

WARNING: Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges, if extra claim charges are authorized.

(x) The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 50-0902, **identifying our Attorney Docket No.** 72255/02661.

(x) 37 CFR 1.16(a), (f), or (g) (filing fees)
(x) 37 CFR 1.16(b), (c) and (d) (presentation of extra claims)
(x) 37 CFR 1.17 (application processing fees)
( ) 37 CFR 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)
( ) 37 CFR 1.17(a)(1)-(5) (extension fees pursuant to 37 CFR 1.136(a))

( ) 37 CFR 1.18 (issue fee at or before mailing Notice of Allowance, pursuant to 37 CFR 1.311(b))

16. Instruction As To Overpayment

() Credit Account No. 50-0902, **identifying our Attorney Docket No. _____.**
(x) Refund

17. Incorporation by reference of added pages

(x) The following pages are incorporated by reference:

(x) "Assignment Cover Letter Accompanying New Application"; number of pages added 3

() Added Pages For Papers Referred To In Item 4 Above; number of pages added

( ) Plus added pages deleting names of inventor(s) named in prior application(s) who is/are no longer inventor(s) of the subject matter claimed in this application; number of pages added_ _____.

(x) no further pages form a part of this Transmittal. The transmittal ends with this page.

Date: September 26, 2000

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DOCKET NO. 72255/02661

DIRECT DATA ROUTING SYSTEM

Field of Invention

The present invention relates generally to a system for routing data, and more particularly to a system for accelerating data transfers by routing data in a unique and efficient manner.

Background of the Invention

A common model for network processing consists of a multi-level approach. This is common in many Ethernet LAN protocols such as IEEE 802.3. The model typically includes 3 major levels, namely a) Top :Logical-Link control; b) Middle: Medium Access Control (MAC); and c) Bottom: Physical interface (PHY).

A wireless LAN configuration compliant to IEEE 802.11 is similar to its wired counterpart and has the same three levels. Traditionally, the top Logical-Link control tasks are handled by software running on a HOST processor. The middle level is the responsibility of a MAC processor, which handles all frame traffic between the HOST and the PHY level.

In a typical wireless local area network (WLAN) configuration, a portable or mobile device (e.g., a laptop personal computer) normally includes a HOST processor and a PCI card or PCMCIA card. On this card resides a Medium Access Control (MAC) processing system, a PHY (physical layer) processing device (e.g., a digital signal processor), and a main memory. The MAC processing system includes a MAC processor (e.g., an embedded processor), which is a multi-functional processor engine responsible for a variety of different processing tasks associated with the wireless communications. The PHY processing device performs such functions as encoding/decoding waveforms.

With wireless local area networks (LANs), high data rates (e.g., 56MB/s or greater) are now attainable using new technologies such as Orthogonal Frequency Division Multiplexing (OFDM), as specified in the latest IEEE wireless standard 802.11b.

The present invention overcomes the slow data transfer rates of prior art data transfer systems to provide a data transfer system that provides the necessary throughput required by the higher data processing rates.

Summary of the Invention

According to one aspect of the present invention there is provided a data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising receiving data from a first processing system which stores the received data into a first memory device, and executing a program instruction on an associated processor to transfers at least a portion of the stored data to a second memory device.

According to another aspect of the present invention there is provided a system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising means for receiving data from a first processing means which stores the received data into a first memory means, and executing a program instruction on an associated processing means to transfer at least a portion of the stored data to a second memory means.

According to another aspect of the present invention there is provided a system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising means for receiving data from a first processing means which stores the received data into a first memory, means for transferring the stored data to a second memory means, and means for

executing a program instruction on an associated processor means to store at least a portion of the data stored in the second memory means to a third memory means.

According to another aspect of the present invention there is provided a method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising a first memory device for storing data received from a first processing system, and an associated processing device for executing a program instruction to transfer at least a portion of the stored data to a second memory device.

According to another aspect of the present invention there is provided a system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising a first memory device for storing data received from a first processing system, a second memory device for receiving the data stored in the first memory device, and an associated processor for executing a memory read instruction to transfer at least a portion of the data stored in the second memory device to a third memory device.

According to another aspect of the present invention there is provided a data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising receiving a data packet from a first processing system, wherein said data packet includes a header portion and a data portion, storing the received data packet into a first memory device, transferring the data portion of the data packet from the first memory device to a third memory device, and executing at least one program instruction on an associated processor to transfer the header portion to a second memory device.

According to another aspect of the present invention there is provided a system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising means for receiving a data packet from a first means for processing, wherein said data packet includes a header

portion and a data portion means for storing the received data packet into a first memory means, means for transferring the data portion to a third memory means, and means for executing at least one program instruction on an associated processor to transfer the header portion to a second memory means.

According to another aspect of the present invention there is provided a system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising a first memory device for storing a data packet received from a first processing system, wherein said data packet includes a header portion and a data portion, an associated processor for executing at least one program instruction to transfer the header portion from the first memory device to a second memory device, and hardware logic enabled by the associated processor to transfer the data portion from the first memory device to a third memory device.

An advantage of the present invention is the provision of a data transfer system which provides more efficient data transfer.

Another advantage of the present invention is the provision of a data transfer system which accelerates data transfer.

Still another advantage of the present invention is the provision of a data transfer system which eliminates intermediate storage steps in a data transfer procedure. This helps to also free up register resources (e.g. general purpose registers) internal to the processor.

Still another advantage of the present invention is the provision of a data transfer system which provides the necessary throughput required by the higher data processing rates attainable using new technologies such as Orthogonal Frequency Division Multiplexing (OFDM), as specified in the latest IEEE wireless standard 802.11b.

Yet another advantage of the present invention is the provision of a data transfer system which includes a data transfer instruction which facilitates fast and efficient data transfers under the direct control of the processor software.

Still other advantages of the invention will become apparent to those skilled in the art upon a reading and understanding of the following detailed description, accompanying drawings and appended claims.

Brief Description of the Drawings

The invention may take physical form in certain parts and arrangements of parts, a preferred embodiment and method of which will be described in detail in this specification and illustrated in the accompanying drawings which form a part hereof, and wherein:

Fig. 1 is a block diagram illustrating data transfer systems according to the prior art;

Fig. 2 is a block diagram illustrating a "receive" data transfer system according to a first embodiment of the present invention;

Fig. 3 is a block diagram illustrating a "receive" data transfer system according to a second embodiment of the present invention; and

Fig. 4 is a block diagram illustrating the data path logic for a "receive" operation according to the first and second embodiments of the present invention.

Detailed Description of the Preferred Embodiment

While the present invention is described herein with particular reference to a "receive" operation (memory write), it should be appreciated that the present invention is also applicable to a "transmit" (memory read) operation. In such case, the data flow direction is reversed from what is illustrated for a "receive" operation.

Referring now to Fig. 1, a prior art data path is shown that is common in many MAC processing systems during a "receive" operation, wherein a PHY data stream is received by the MAC processing system. As noted above, the data flow is similar for a "transmit" operation, except the data direction is reversed everywhere.

MAC processing system 10 is generally comprised of an MDI (modem data interface) FIFO memory 20, a MAC processor 30, and a HOST FIFO memory 40. MAC processor 30 includes general purpose registers 32. In accordance with a typical MAC processing system, a PHY processing system 5 (e.g., an RF physical layer (PHY) processing device) transmits a PHY data stream that arrives at MAC processing system 10 as a plurality of packets (or frames) in a byte-wise fashion. It should be appreciated that FIFO memories are needed to interface with MAC processor 30 and HOST processor 60, since data rates may differ significantly between a PHY data processing system and the HOST processor. Furthermore, HOST processor 60 may be working on different packet than the packet of the PHY data stream transferring between PHY data processing system 5 and MAC processor 30. Also, the PHY data stream and the data processed by HOST processor 60 tend to be bursty in nature. Consequently, data arrives at a non-uniform data rate and thus requires a FIFO memory to synchronize the data traffic between PHY data processing system 5 and HOST processor 60. Therefore, the PHY data processing system, MAC processor 30 and HOST processor 60 operate independently of each other to form a loosely coupled system, which requires FIFOs for coordination and synchronization.

The packets comprising the PHY data stream have two main components, namely, a header portion, and a data portion. The header portion includes control information such as source, destination address; data rate, etc. It is important for MAC processor 30 to process the header information quickly so it knows how to deal with the data portion. Furthermore, some information in the header may direct MAC processor 30 to perform other actions, such as generating a response message to the sender or steering

the data to another station. The data portion includes data (usually encrypted) for HOST processor 60. This data may be used by HOST processor 60 to communicate with other HOSTs across a network using some upper level protocol. Sending an FTP from one station to another station is one such example. In the case of a system complying with IEEE 802.11, HOST processor 60 does not use the 802.11 header information, as it is only used by MAC processor 30.

The PHY data is held in intermediate storage in MDI FIFO memory 20, before being transferred to MAC processor 30 for further processing. It should be understood that the PHY data may require alignment by hardware from MAC FIFO memory 20 into a data pattern compatible with MAC processor 30 (e.g., 16-bit or 32-bit words), so that MAC processor 30 can proceed with further processing of the PHY data. MAC processor 30 moves the PHY data stored in MDI FIFO memory 20 to general purpose registers 32 of MAC processor 30 for further processing. After processing by MAC processor 30, the data is typically stored as a data structure (e.g., chained buffer) residing in off-chip MAIN memory 50 as packets or frames. Later, the stored data is accessed by HOST processor 60, under the direction of MAC processor 30.

It should be appreciated that many typical MAC processing systems include a FIFO memory (e.g., MDI FIFO memory 20) so that received data can be queued up for processing by the MAC processor. This queuing process allows the received PHY data to be synchronized and properly formatted for later use when the MAC processor has time to process the data. Moreover, to transfer data one block at a time between general purpose registers 32 and main memory 50, MAC processor 30 executes a program instruction, such as "Move FIFO to Register." Therefore, the program instruction code for transferring the received data between MDI FIFO memory 20 and MAIN memory 50 may be as follows:

```
MOV   RXHR, R1      ; Move contents of holding register of FIFO 20 to
                      General Register R1 of MAC processor 30
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MWR R2+, R1 ; Write contents of General Register R1 to MAIN Memory 50; post-increment Address Pointer R2

Accordingly, the corresponding register transfer level description is as follows:

cycle 1: R1 ⇐ $FIFO_{holding\ register}$	move contents of Holding Register of FIFO 20 to General Register R1 of MAC processor 30
cycle 2: Mem[R2] ⇐ R1	Write contents of General Register R1 of MAC processor 30 to the memory address of MAIN memory 50, stored in Register R2

Likewise, on "transmit" the program instruction code for transferring data from MAIN memory 50 to the transmit MDI FIFO memory 20 is as follows:

MRD R2+,R1	Read contents of MAIN Memory 50 and store into General Register R1 of MAC processor 30; post-increment Address Pointer R2
MOV R1,TXHR	Move contents of General Register R1 of MAC processor 30 to holding register of FIFO 20

Accordingly, the corresponding register transfer level description is as follows:

cycle 1: R1 ⇐ MEM[R2]	Read contents of memory address [R2] into General Register R1 of MAC processor 30
cycle 2: $FIFO_{holding\ register}$ ⇐ R1	Move contents of General Register R1 into FIFO holding register

Thus, in accordance with the prior art, a total of two instructions are needed to transfer data to MDI FIFO memory 20 from MAIN memory 50. Thus, on "receive" it requires two instructions to perform this: (1) Fetch MOV (move) instruction, and (2) Fetch MWR (memory write) instruction. It should be appreciated that this may require 3 clock cycles

on processors that have a shared data and instruction bus (vonNewman architecture), or where data dependencies in the register transfers require the processor to stall between operations.

Another prior art approach has been to use a direct memory access (DMA) function to allow hardware to move data directly from MDI FIFO memory 20 into MAIN memory 50, as also illustrated by Fig. 1. This is very efficient, since MAC processor 30 is not involved in the data transfer. However, it has a disadvantage in that MAC processor 30 loses track of the data transfer. Since the DMA activity is done by hardware, it is non-deterministic and asynchronous with respect to MAC processor 30. Therefore, MAC processor 30 is completely unaware of data movement, or even the sequence of the byte stream movement. With the protocol for wireless LANs specified by IEEE standard 802.11, it is important for MAC processor 30 to be aware of where it stands in the byte stream. This is due to the fact that IEEE 802.11 demands on the MAC processor force it to coordinate and process the data frames on a timely basis. This forces the software running on MAC processor 30 to be flexible and aware of the different types of incoming frames so it can quickly react.

DMA has other drawbacks in that typically the data is sent as a burst of consecutive bytes. This can adversely effect the MAC processor as it performs critical actions due to the additional memory traffic caused by the DMA. This may block the MAC processor from accessing the MAIN memory for other reasons while the DMA is in progress for lengthy periods of time. For example, in the case of a full duplex system (i.e., a system capable of transmitting and receiving data simultaneously), the MAC processor might be busy transmitting an important control frame to the PHY processing system. At the same time during a MAC processor receive, a MDI FIFO 20 to MAIN memory 50 DMA may cause the MAC processor to underrun on the transmit control frame. There is no way for the MAC processor to coordinate and control the DMA since it is all done by hardware. It should be understood that the present invention is applicable

to a full duplex system wherein the MAC processor is capable of full duplex transfers. In full duplex, data is simultaneously transmitted and received between the MAC processor 30 and MDI FIFO 20, and between MAC processor 30 and MAIN memory 50.

Referring now to Fig. 2, the present invention provides a special instruction to move data directly from MDI FIFO memory 20 to a MAIN memory 50, without the need for any transfer to an intermediate register (i.e., general purpose registers 32 of MAC processor 30). As indicated above, prior art approaches to data routing require two instructions to transfer data from MDI FIFO memory 20 to the MAIN memory 50. In accordance with a first embodiment of the present invention, there is provided an instruction function in which hardware allows a direct data transfer between MDI FIFO memory 20 and MAIN memory 50. This instruction function results in program code that is more efficient than the prior art program code described above. Exemplary program code is as follows:

Receive Operation:

```
MWR  R2+, RXHR    ; Write contents of MDI FIFO memory 20 to
                    MAIN Memory 50; Post Increment Address
                    Pointer R2
```

Transmit Operation:

```
MRD  R2+, TXHR    ; Read contents of MAIN Memory 50 into MDI
                    FIFO memory 20; Post Increment Address
                    Pointer R2
```

Accordingly, the corresponding register transfer level description is as follows:

Receive Operation:

cycle 1: $Mem[R2] \Leftarrow FIFO_{\text{holding register}}$ Write contents of Holding Register FIFO to memory address of MAIN memory 50 stored in Register R2

Transmit Operation:

cycle 1: $FIFO_{holding\ register} \Leftarrow Mem[R2]$	Read contents of memory address of MAIN memory 50 stored in Register R2 into the Holding Register FIFO

Therefore, a total of one instruction is needed to effect a transfer of data from MDI FIFO memory 20 to MAIN memory 50. Consequently, only one clock cycle is needed to execute the data transfer: (1) Fetch memory write instruction (MWR). It should be appreciated that this may require two clock cycles on processors that have a shared data and instruction bus (vonNewman architecture). However, there are no additional cycles (stall cycles) needed for data dependencies in the register transfers which may be required for some computer architectures using the prior art approach.

Fig. 2 illustrates the data path, wherein data merely passes through MAC processor 30 on route to MAIN memory 50, rather than being stored in an associated general purpose register. Subsequently, the data is transferred from MAIN memory 50 to HOST FIFO memory 40 via a hardware driven operation, such as a DMA function.

The new instruction function described above provides the control for directing the datapath shown in Fig. 2 to perform the direct data transfer from MDI FIFO 20 to MAIN memory 50. Since the implementation is performed using software control (i.e., the FIFO/Memory transfer instructions described above), it still provides firmware with the ability to react to the PHY data stream on a timely basis, unlike DMA.

MAC processor 30 will commonly process the entire frame (i.e., header portion and data portion) into MAIN memory 50. The data portion of this frame is formatted by MAC processor 30 to be later sent to HOST processor 60 via HOST FIFO 40 using a Host protocol (e.g., PCI bus). A DMA hardware-based engine is suitable for this action since a burst of data traffic is the preferred means of transferring data across a PCI bus. There is no need for HOST processor 60 to be aware of all data movement, an "interrupt" indicating when the block has been completely sent is one suitable solution.

In this regard, HOST processor 60 does not need to react as quickly, since the timing for HOST processor 60 is much more relaxed compared to the tight timing MAC processor 30 must meet to comply with a communications protocol, such as IEEE 802.11b.

In accordance with a second embodiment of the present invention, data transfers (i.e., the data portion of the frame) between MDI FIFO memory 20 and MAIN memory 50 are eliminated, as will now be described with reference to Fig. 3. A direct access path from MDI FIFO memory 20 to HOST FIFO memory 40 is provided . This provides significant improvements in efficiency, i.e., even better than a DMA transfer, since intermediate storage in the MAIN memory 50 is eliminated. The improvement in throughput, power, memory space, etc. is obvious using this technique.

In the second embodiment of the present invention, MAC processor 30 processes the data in two phases. First, the header portion of the frame (or packet) is processed by MAC processor 30, as described in connection with the first embodiment described above. However, after the header portion has been processed by MAC processor 30, the data portion of the frame (or packet) is transferred directly from MDI FIFO 20 to HOST FIFO 40, without any intermediate transfer to MAIN memory 50. This path is enabled under the direction of the MAC processor software using a configuration register. The header portion is subsequently transferred from MAC processor 30 to MAIN memory 50. It should be understood that a configuration bit is set by MAC processor 30 in order to enable the direct data transfer path between MDI FIFO 20 and HOST FIFO 40. No program instructions are required to enable this data transfer mode.

It should be understood that the direct data stream from MIDI FIFO 20 to HOST FIFO 40 should be carefully controlled, and may be useful only on certain frames; since MAC processor intervention is needed in many cases. On most frames it is not useful since MAC processor 30 must react and process the data on a timely basis. This is required since it is not possible to deterministically predict the contents of forthcoming frames. However, in cases where data arrives in a streaming fashion (e.g., Video or

Audio data) this second embodiment can be used as an optimization. This is the case in applications such as wireless bridging devices, where a direct data transfer occurs repetitively and is more predictable. Thus, it may be preferable to utilize the second embodiment (for streaming type data frames) of the present invention in combination with the first embodiment (for other data frames and control frames) of the present invention.

One approach is to process a "lead frame" indicating to MAC processor 30 how many streamed data frames will be arriving next. At that point, MAC processor 30 knows to enable the "direct data mode" of the second embodiment, since there is a priori knowledge and predictability in the forthcoming data stream. The added advantage of this approach is not only speed and reduced memory traffic, but lower latency; since HOST processor 60 can react to the incoming data as soon as possible. This provides improved quality of service for fast PHY data to HOST data requirements found in wireless voice and video image applications where low latency is important.

Referring now to Fig. 4, there is shown the data path logic for a "receive" frame operation (FIFO to MEMORY), according to the first and second embodiments of the present invention. The dashed lines show the data path logic specific to the second embodiment. Referring to the first embodiment, the FIFO to MEMORY instruction (MRW - memory read) is fetched and decoded using instruction register 100 and instruction decode logic 110. When it executes, the data output MUX 150 is enabled to write data from the FIFO holding register 140 to off-chip MAIN memory 50. Also, the execute advances FIFO pointer logic 120 to align and load the next FIFO data location into FIFO holding register 140 for the next transfer. When the second embodiment is enabled by MAC processor 30, the data portion of the frame is sent directly from holding register 140 of MDI FIFO 20 to the HOST FIFO 40, with no further processor intervention or memory traffic. The header portion of the frame proceeds to MAIN memory 50 as in the first embodiment.

The present invention has been described with reference to a preferred embodiment. Obviously, modifications and alterations will occur to others upon a reading and understanding of this specification. It is intended that all such modifications and alterations be included insofar as they come within the scope of the appended claims or the equivalents thereof.

Having thus described the invention, it is now claimed:

1. A data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising:

receiving data from a first processing system;

storing the received data into a first memory device; and

executing a program instruction on an associated processor to transfer at least a portion of the stored data to a second memory device.

2. A data transfer method according to claim 1, wherein said method further comprises:

transferring at least a portion of the data stored in said second memory device to a third memory device, wherein said second processing system operates upon the data stored in said third memory device.

3. A data transfer method according to claim 1, wherein said first memory device is a FIFO memory device.

4. A data transfer method according to claim 1, wherein said third memory device is a FIFO memory device.

5. A data transfer method according to claim 1, wherein method further comprises byte-aligning the data stored in said first memory device.

6. A data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising:

receiving data from a first processing system;

storing the received data into a first memory device;

transferring the stored data to a second memory device; and

executing a program instruction on an associated processor to store at least a portion of the data stored in the second memory device to a third memory device.

7. A data transfer method according to claim 6, wherein said second processing system operates upon the data stored in said third memory device.

8. A data transfer method according to claim 6, wherein said first memory device is a FIFO memory device.

9. A data transfer method according to claim 6, wherein said third memory device is a FIFO memory device.

10. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

means for receiving data from a first processing means;

means for storing the received data into a first memory means; and

executing a program instruction on an associated processing means to transfer at least a portion of the stored data to a second memory means.

11. A system according to claim 10, wherein said system further comprises:

means for transferring at least a portion of the data stored in said second memory means to a third memory means, wherein said second processing means operates upon the data stored in said third memory means.

12. A system according to claim 10, wherein said first memory means is a FIFO memory device.

13. A system according to claim 10, wherein said third memory means is a FIFO memory device.

14. A system according to claim 10, wherein system further comprises means for byte-aligning the data stored in said first memory means.

15. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

means for receiving data from a first processing means;

means for storing the received data into a first memory means;

means for transferring the stored data to a second memory means; and

means for executing a program instruction on an associated processor means to store at least a portion of the data stored in the second memory means to a third memory means.

16. A system according to claim 15, wherein said second processing means operates upon the data stored in said third memory means.

17. A system according to claim 15, wherein said first memory means is a FIFO memory device.

18. A system according to claim 15, wherein said third memory means is a FIFO memory device.

19. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

a first memory device for storing data received from a first processing system; and

an associated processing device for executing a program instruction to transfers at least a portion of the stored data to a second memory device.

20. A system according to claim 19, wherein said system further comprises hardware logic for transferring at least a portion of the data stored in said second memory device to a third memory device, wherein a second processing system operates upon the data stored in said third memory device.

21. A system according to claim 19, wherein said first memory device is a FIFO memory.

22. A system according to claim 19, wherein said third memory device is a FIFO memory.

23. A system according to claim 19, wherein said first memory device byte-aligns the data stored therein.

24. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

a first memory device for storing data received from a first processing system;

a second memory device for receiving the data stored in the first memory device; and

an associated processor for executing a memory read instruction to transfer at least a portion of the data stored in the second memory device to a third memory device.

25. A system according to claim 24, wherein said system further comprises a second processing system for operating upon the data stored in said third memory device.

26. A system according to claim 24, , wherein said first memory device is a FIFO memory.

27. A system according to claim 24, wherein said third memory device is a FIFO memory.

28. A data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising:

receiving a data packet from a first processing system, wherein said data packet includes a header portion and a data portion;

storing the received data packet into a first memory device;

transferring the data portion of the data packet from the first memory device to a third memory device; and

executing at least one program instruction on an associated processor to transfer the header portion to a second memory device.

29. A data transfer method according to claim 28, wherein a second processing system operates upon the data portion stored in said third memory device.

30. A data transfer method according to claim 28, wherein said first memory device is a FIFO memory device.

31. A data transfer method according to claim 28, wherein said third memory device is a FIFO memory device.

32. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

means for receiving a data packet from a first means for processing, wherein said data packet includes a header portion and a data portion;

means for storing the received data packet into a first memory means;

means for transferring the data portion to a third memory means; and

means for executing at least one program instruction on an associated processor to transfer the header portion to a second memory means.

33. A system according to claim 32, wherein a second means for processing operates upon the data portion stored in said third memory means.

34. A system according to claim 32, wherein said first memory means is a FIFO memory device.

35. A system according to claim 32, wherein said third memory means is a FIFO memory device.

36. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

a first memory device for storing a data packet received from a first processing system, wherein said data packet includes a header portion and a data portion;

an associated processor for executing at least one program instruction on to transfer the header portion from the first memory device to a second memory device; and

hardware logic enabled by the associated processor to transfer the data portion from the first memory device to a third memory device.

37. A system according to claim 36, wherein said system further comprises a second processing system for operating upon the data stored in said third memory device.

38. A system according to claim 36, wherein said first memory device is a FIFO memory.

39. A system according to claim 36, wherein said third memory device is a FIFO memory.

40. A data processing system comprising:

a processor for transferring data to a memory location identified by an address stored in an address pointer register;

a FIFO memory for storing data; and

a first memory for storing data at a plurality of memory locations, each memory location identified by an address,

wherein the processor receives an instruction to transfer data from the FIFO memory to a memory location of the first memory identified by the address stored in the address pointer register, and automatically increments the address stored in the address pointer register to identify another memory location of the first memory, said instruction having a first parameter identifying the address pointer register, and a second parameter identifying the first memory.

41. A data processing system comprising:

a processor for transferring data from a memory location identified by an address stored in an address pointer register;

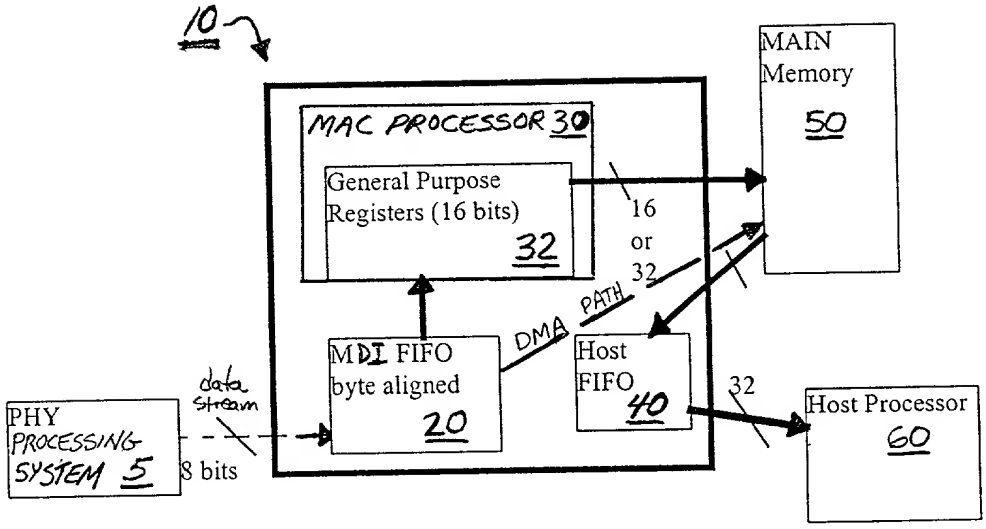
a first memory for storing data at a plurality of memory locations, each memory location identified by an address; and

a FIFO memory for storing data,

wherein the processor receives an instruction to transfer data from a memory location of the first memory identified by the address stored in the address pointer register to the FIFO memory, and automatically increments the address stored in the address pointer register to identify another memory location of the first memory, said instruction having a first parameter identifying the address pointer register, and a second parameter identifying the FIFO memory.

ABSTRACT

A system of data transfer between a first processing device and a second processing device which speeds data transfer by eliminating intermediate storage steps. A plurality of memory storage devices are provided between the first and second processing devices for the purpose of synchronization and alignment. One of the memory storage devices is associated with the second processing device. In accordance with a first embodiment of the present invention, a new instruction is provided to implement a data transfer function for transferring data directly between a first memory storage device and a second memory storage device, without intermediate storage in a processor register. Thereafter, the data is transferred from the second memory storage device to the memory storage device associated with the second processing device. In accordance with a second embodiment of the present invention, data is efficiently transferred directly between a first memory storage device and the memory storage device associated with the second processing device, without intermediate storage in either a processor register or a second memory storage device.



PRIOR ART

Fig. 1

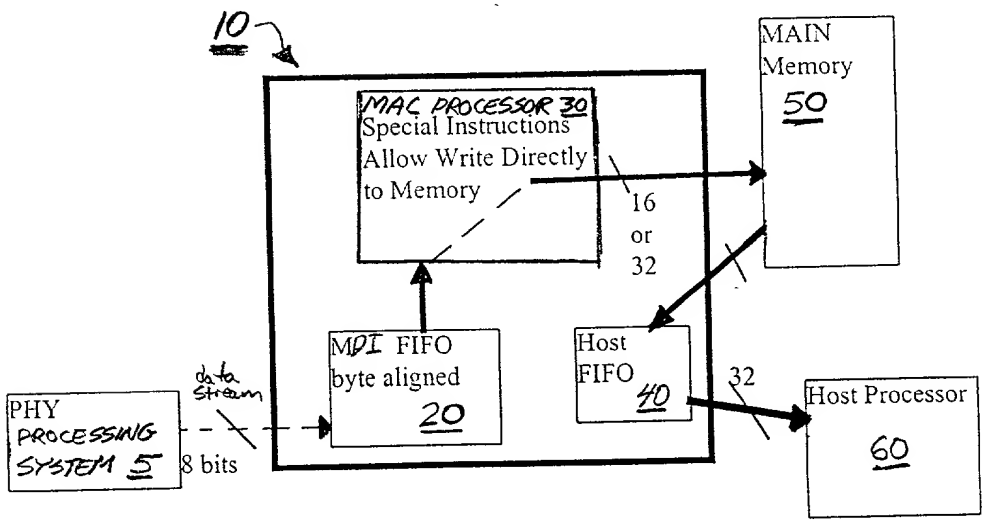


Fig. 2

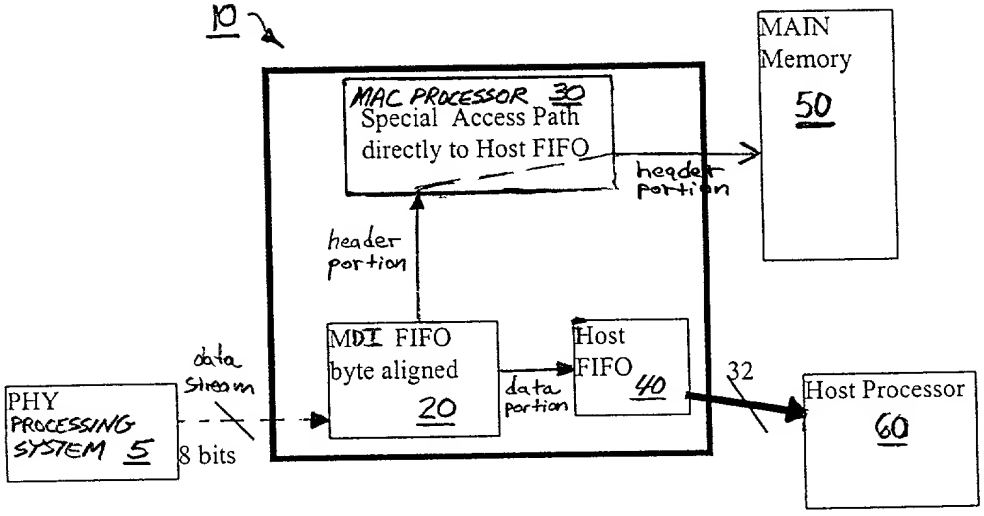

10
MAC PROCESSOR 30
Special Access Path
directly to Host FIFO
MAIN
Memory
50
header portion
header portion
MDI FIFO
byte aligned
20
Host
FIFO 40
data portion
32
Host Processor
60
data stream
PHY
PROCESSING
SYSTEM 5
8 bits

Fig. 3

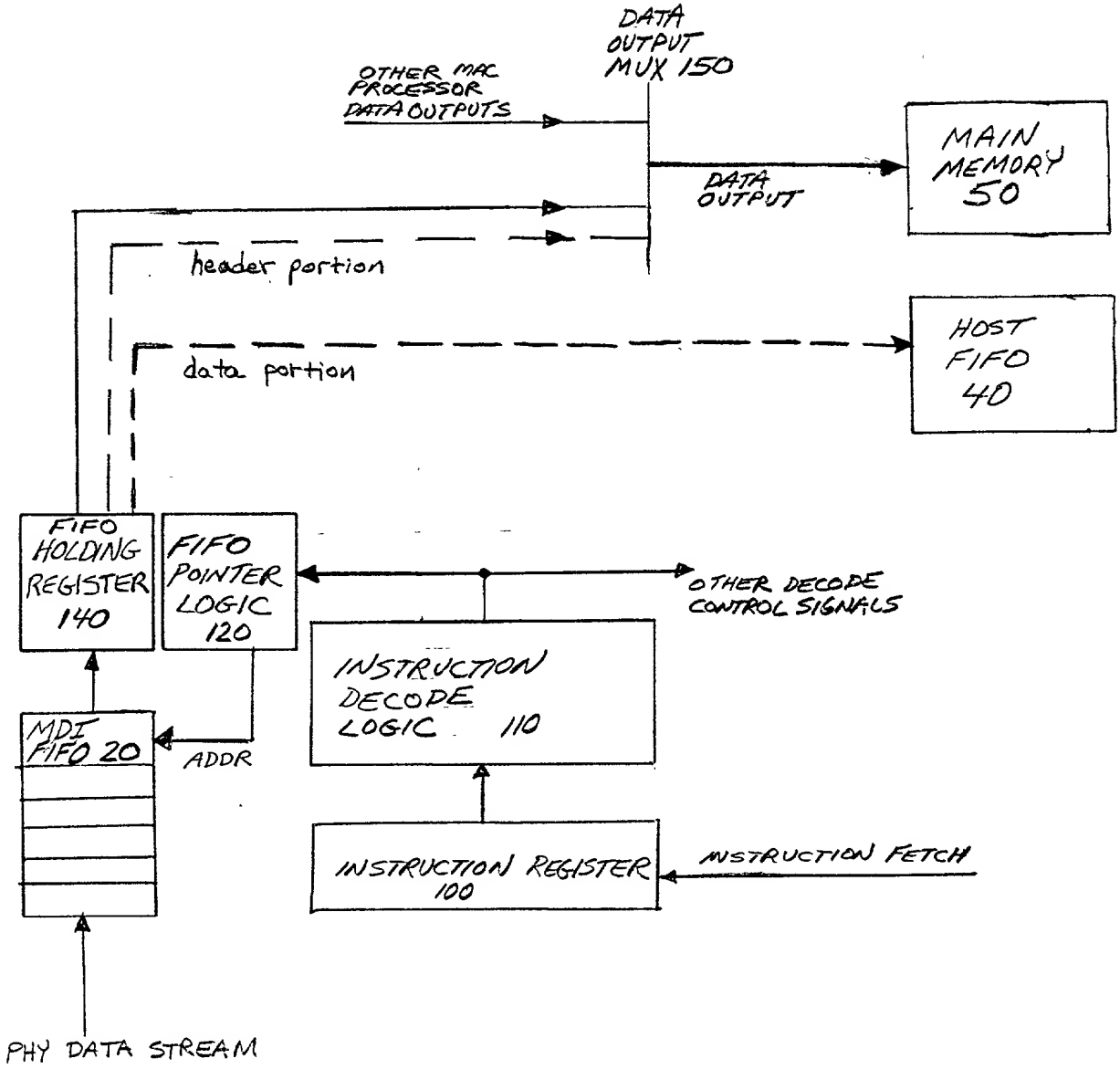

DATA OUTPUT MUX 150
OTHER MAC PROCESSOR DATA OUTPUTS
MAIN MEMORY 50
DATA OUTPUT
header portion
data portion
HOST FIFO 40
FIFO HOLDING REGISTER 140
FIFO POINTER LOGIC 120
OTHER DECODE CONTROL SIGNALS
INSTRUCTION DECODE LOGIC 110
MDI FIFO 20
ADDR
INSTRUCTION REGISTER 100
INSTRUCTION FETCH
PHY DATA STREAM

Fig. 4

Docket No. 72255/02661

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed, and for which a patent is sought on the invention entitled:

DIRECT DATA ROUTING SYSTEM

the specification of which is attached hereto, unless the following box is checked:

___ was filed on _____, 20___, as United States Application Number or PCT International Application Number _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §§119(a) - (d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

NONE

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

NONE

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose

information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

NONE

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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